IN THE CLAIMS

1. (Currently Amended) A clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter for delivering a total count value by counting the total number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter for delivering a difference value obtained by subtracting either the total count value or a reference value from the other;

a control voltage generation circuit for delivering an analog control voltage corresponding to an integrated value of the difference value obtained by adding a new difference value to the stored integrated value; and

a voltage control oscillator circuit for delivering the output clock signal at a frequency corresponding to the analog control voltage,

wherein the counter is a counter for delivering the total count value by counting the total number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is only at a High level, and

the counter, the subtracter, the control voltage generation circuit, and the voltage control oscillator circuit having response characteristics such that when the total count value is changed from a preceding total count value, the frequency of the output clock signal is changed during a period in which the reference clock signal is a Low level, after the end of the counting period and before the start of a succeeding counting period.

2. (Canceled).

3. (Currently Amended) A clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter for delivering a total count value by counting the total number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter for delivering a difference value obtained by subtracting either the total count value or a reference value from the other;

a control voltage generation circuit for delivering an analog control voltage corresponding to an integrated value of the difference value obtained by adding a new difference value to the stored integrated value; and

a voltage control oscillator circuit for delivering the output clock signal at a frequency corresponding to the analog control voltage,

wherein the counter is a counter for obtaining the total count value at the end of each High level period and each Low level period of the reference clock signal, and

the counter, the subtracter, the control voltage generation circuit and the voltage control oscillator circuit having response characteristics in which when the total count value obtained by counting during a High level period of the reference clock signal is changed from a preceding total count value, the frequency of the output clock signal is changed ~~from a preceding count value, the frequency of the output clock signal is~~

~~changed~~ after the end of the High level period of the reference clock signal and before the start of the next High level period of the reference clock signal and the characteristics in which when the total count value obtained by counting during a Low level period of the reference clock signal is changed from a preceding total count value, the frequency of the output clock signal is changed after the end of the Low level period of the reference signal and before the start of the ~~succeeding~~ next Low level period of the reference signal.

4. (Canceled).

5. (Currently Amended) A clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter for delivering a total count value by counting the total number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter for delivering a difference value obtained by subtracting either the total count value or a reference value from the other;

a control voltage generation circuit for delivering an analog control voltage corresponding to an integrated value of the difference value obtained by adding a new difference value to the stored integrated value; and

a voltage control oscillator circuit for delivering the output clock signal at a frequency corresponding to the analog control voltage,

wherein the counter delivers the total count value after the end of the counting period and in synchronization with the output clock signal, the subtracter generates a difference value in sync with an output clock signal generated after the counter generates a total count value in sync with an output clock signal, the control voltage generation circuit generates an analog control signal in sync with an output clock signal generated after the subtracter generates the difference value in sync with the output clock signal.

6. (Currently Amended) A clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter for delivering a total count value by counting the total number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter for delivering a difference value obtained by subtracting either the total count value or a reference value from the other;

a control voltage generation circuit for delivering an analog control voltage corresponding to an integrated value of the difference value; and

a voltage control oscillator circuit for delivering the output clock signal at a frequency corresponding to the analog control voltage,

wherein the counter counts each rising edge at which the output clock signal transmits from a Low level to a High level and each falling edge at which the output

clock signal transmits from the High level to the Low level as the effective transition edges of the output clock signal.

7. (Currently Amended) A clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter for delivering a total count value by counting the total number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter for delivering a difference value obtained by subtracting either the total count value or a reference value from the other;

a control voltage generation circuit for delivering an analog control voltage corresponding to an integrated value of the difference value; and

a voltage control oscillator circuit for delivering the output clock signal at a frequency corresponding to the analog control voltage,

wherein a multiplier for multiplying the difference value by a predetermined factor and delivering a multiplied difference value to the control voltage generation circuit is interposed between the subtracter and the control voltage generation circuit.

8. (Original) A clock multiplication circuit according to claim 7,

wherein the multiplier comprised of a shift register for implementing bit shift of the difference value by predetermined bits.

9. (Original) A clock multiplication circuit according to claim 7, wherein a factor of the multiplier is variable.

10. (Original) A clock multiplication circuit according to claim 9, further comprising factor control means for controlling the factor of the multiplier, the factor control means being capable of raising the factor to a relatively high number during a lock-in period, and lowering the factor to a relatively low number after the end of the lock-in period.

11. (Currently Amended) A clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter for delivering a total count value by counting the total number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter for delivering a difference value obtained by subtracting either the total count value or a subtracter reference value from the other;

a control voltage generation circuit for delivering an analog control voltage corresponding to an integrated value of the difference value; and

a voltage control oscillator circuit for delivering the output clock signal at a frequency corresponding to the analog control voltage,

wherein the subtracter is capable of switching the subtracter reference value.

12. (Previously Presented) A clock multiplication circuit according to claim 11,

wherein the subtracter comprises reference value storage means for storing the subtracter reference value, the reference value storage means configured so as to enable the subtracter reference value to be stored in the reference value storage means from outside.

Claims 13-22. (Canceled).

Claim 23. (Currently Amended) A clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter for delivering a total count value by counting the total number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter for delivering a difference value obtained by subtracting either the total count value or a reference value from the other;

a control voltage generation circuit for delivering an analog control voltage corresponding to an integrated value of the difference value obtained by adding a new difference value to the stored integrated value; and

a voltage control oscillator circuit for delivering the output clock signal at a frequency corresponding to the analog control voltage,

wherein the counter is a counter for delivering the total count value by counting the total number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is only at a Low level, and

the counter, the subtracter, the control voltage generation circuit, and the voltage control oscillator circuit having response characteristics such that when the total count value is changed from a preceding total count value, the frequency of the output clock signal is changed during a period in which the reference clock signal is a High level, after the end of the counting period and before the start of a succeeding counting period.